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Article in Journal of Low Power Electronics - March 2018
DOI: 10.1166/jolpe.2018.1529

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Design and Power Analysis of New Coplanar One-Bit Full-Adder Cell in Quantum-Dot Cellular Automata

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(Received: 14 October 2017; Accepted: xx Xxxx xxxx)

Quantum-dot cellular automata is one of the most important emerging technologies for designing nano-electronic circuits. One of the essential functions in arithmetic circuits is the one-bit full-adder cell. Moreover, in QCA field coplanar architectures are very important because using this approach, we can simplify the implementation of this function. In this paper, a new single layer full-adder cell is introduced based on difference phase application. We have achieved significant improvements in terms of complexity, area and power consumption. Particularly simulation results show 2.43% and 24.24% as well as (27.54% in 0.5 EK, 23.61% in 1 EK and 21.02% in 1.5 EK) reduction respectively in complexity and area overhead as well as power consumption. We have also proposed a novel coplanar 2-input XOR gate based on the proposed full-adder cell. Although, the main idea in this paper is just evaluating how we can implement a low power one-bit full-adder cell.

Keywords: Quantum-Dot Cellular Automata (QCA), Full-Adder Cell, Power Consumption, Arithmetic Circuit, XOR Gate.

1. INTRODUCTION

Quantum-dot cellular automata (QCA) technology is one of the most important suitable nano-electronic technologies which has been introduced as a possible replacement of CMOS-based devices.¹,² Because CMOS-based technologies have many serious disadvantages which include short channel effect, impurity variations, a high cost of lithography and more importantly, the heat. Recently many have focused on new technologies.³–⁵ On the other hand, QCA has attracted much more attention because it has many advantages, such as ultra-low-energy consumption, fast operation and high device density.⁶

Generally, the QCA is divided into 4 types; Metal-Island, Semiconductor, Magnetic and Molecular where Metal-Island as well as, semiconductor types are based on silicon. In order to implement molecular types, one based on graphene has attracted attention.⁷ Our proposed work is suitable for using in Semiconductor and Metal Island types. Since in these types, their cell instructors are in square shape, but other types of QCA such as Magnetic and Molecular in general implement with a rectangular shape. Moreover, QCADesigner tool works based on Semiconductor type. So we just can simulate this type. With the use of QCA cell, we are able to encode binary information, so this structure is suitable for binary computation because in every cell there are 4 quantum dots which can provide two types of codings.⁸,⁹

The adder cell is an essential element in the design of arithmetic circuits based on QCA technology. In other words, efficient design of the new adder cell can be applied most effectively for the entire system. One can achieve many improvements in different parameters. In addition, as in VLSI circuits speed, area and power are the most important performance evaluation parameters.¹⁰ In order to provide a comprehensive analysis, in this study, energy dissipation analysis is also calculated.

In this study, we propose an area and energy efficient one-bit coplanar full-adder cell. The modified design provides many advantages including single layer implementation, lower energy dissipation, lower number of cells and smaller area.

The remainder of this paper is organized as follows: The QCA fundamentals and the related works are reviewed in the Sections 2 and 3, respectively. Section 4 provides definitions of the proposed method. Simulation results and comparisons are presented in Section 5. Finally, Section 6 concludes the paper.

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2. QCA FUNDAMENTALS

2.1. QCA Cells and Logic Gates

The basic QCA cell is illustrated in Figure 1. Each cell consists of four quantum dots and is occupied by one pair of electrons. Considering the Coulombic interaction between electrons in each cell, they are placed at diagonally opposite positions. Regarding the high inter-cell potential, they cannot tunnel between neighbouring cells. Therefore, there are two configurations in every cell whose polarizations are $-1$ and $+1$ and are symbolized by binary values of 0 and 1.\textsuperscript{11,12}

In the QCA field, there are two methods for implementation of a binary wire. One is based on 90-degree cells and the other is based on 45-degree cells. Each type consists of a number of cells that propagate an input logic value to the output cell by the Coulombic energy transaction between the electrons of the array cells. These two types of QCA wires are illustrated in Figure 2.\textsuperscript{13}

Generally, there are two kinds of QCA inverters as shown in Figure 3. Considering the general rule about an inverter gate after applying the value to the input cell, the output cell produces the reverse value.\textsuperscript{13}

The basic QCA majority gate is depicted in Figure 4. Each 3-input majority gate consists of a 3 input cells, one voter cell, and one output cell. If two or more input values equal logic “1” output value produces the logic “1”, otherwise it produces the logic “0”. So the functionality of a 3-input majority gate is given by Eq. (1).\textsuperscript{13}

$$M(A, B, C) = AB + BC + AC$$ (1)

2.2. Cross Wire Approaches

In QCA field, there are three types of cross wire including Multi-Layer, Coplanar, and Coplanar clocking based.
Although the implementation of Multi-Layer in QCA field is impractical because until now the researchers have not been able to introduce a solution that can allow for communication between layers. Thus, regarding the importance of implementing single-layer in this paper, manners to help develop single layer designs are described. For the implementation, the rotated manner uses a two-wire, one of which is based on 90-degree cells and the other wire is based on 45-degree. The structure of this manner is shown in Figure 5(a). Furthermore, to implement the Coplanar clocking based manner, we must design every one of the two cross wires with a zero or two QCA clock phases or they must implement with a one or three QCA clock phases. In Figure 5(b), the example of this manner is depicted.\textsuperscript{14}

Fig. 6. The presented full-adders in (a) Ref. [24] (b) Ref. [25] (c) Ref. [26] (d) Ref. [27] (e) Ref. [28].

![Diagram of full-adder cells](image)

Fig. 7. The proposed full-adder cell.
Table I. Power analysis results of inverter gates.

<table>
<thead>
<tr>
<th>Proposed circuits</th>
<th>Avg. leakage energy dissipation (meV)</th>
<th>Avg. switching energy dissipation (meV)</th>
<th>Total energy consumption (meV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.5 EK</td>
<td>1 EK</td>
<td>1.5 EK</td>
</tr>
<tr>
<td>Corner approach</td>
<td>0.00194</td>
<td>0.00425</td>
<td>0.00652</td>
</tr>
<tr>
<td>Robust design</td>
<td>0.00251</td>
<td>0.00728</td>
<td>0.01258</td>
</tr>
</tbody>
</table>

2.3. Kink Energy

Power in Quantum-dot cellular automata calculates by means of the Coulombic interaction between cells. This concept is modelling with Eq. (2).

\[
H = \frac{-E_K}{2} \sum_i C_i f_{i,j} - \gamma \\
-\gamma \frac{E_K}{2} \sum_i C_i f_{i,j}
\]

\[
= \frac{-E_K}{2} (C_{j-1} + C_{j+1}) - \gamma \\
-\gamma \frac{E_K}{2} (C_{j-1} + C_{j+1})
\]

In Eq. (2) \(C_i\) is the polarization of the \(i\)th juxtaposed cell and \(f_{i,j}\) is the geometrical factor which determines the electrostatic interaction between cells \((i\) and \(j)\), considering the geometrical distance. So in the situation of where the neighboring cells are equally spaced, factor \(f_{i,j}\) is absorbed into the Kink energy definition \((E_k)\). This energy is affiliated with the energy cost of two QCA cells \((i\) and \(j)\) with different polarizations and can be computed as

\[
E_{i,j} = \frac{1}{41E_{0}\epsilon} \sum_{i=1}^{4} \sum_{m=1}^{4} q_{i,n} q_{j,n} r_{i,n} - r_{j,n}
\]

The QCA cell energy at each clock cycle is calculated as

\[
E = \langle H \rangle = \frac{\hbar}{2} \vec{I} \cdot \vec{\Lambda}
\]

Which \(\vec{I}\) is the energy vector of the cell that holds its neighbors effects, \(\hbar\) is reduced Planck constant and \(\vec{\Lambda}\) represents Coherence vector. The Hamiltonian is given by Eq. (5)

\[
\vec{I} = \frac{1}{\hbar} \left[ -2\gamma, 0, E_K (C_{j-1} + C_{j+1}) \right]
\]

Which \((C_{j-1} + C_{j+1})\) is the sum of the neighboring polarizations. Considering the mentioned concepts, the author of Ref. [21] introduced QCAPro tool. In general,
Table II. Characteristics analysis of the single layer full-adders and 2-input XOR.

<table>
<thead>
<tr>
<th>Design</th>
<th>Number of fixed cells</th>
<th>Fixed polarities</th>
<th>Number of cells</th>
<th>Latency (number of clock cycles)</th>
<th>Crossover type</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-adder</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ref. [9]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>190</td>
<td>Without clocking</td>
<td>Coplanar (rotated cells)</td>
<td>0.2</td>
</tr>
<tr>
<td>Ref. [15]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>145</td>
<td>1</td>
<td>Coplanar (rotated cells)</td>
<td>0.16</td>
</tr>
<tr>
<td>Ref. [18]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>95</td>
<td>1.25</td>
<td>Coplanar (clocking based)</td>
<td>0.09</td>
</tr>
<tr>
<td>Ref. [22]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>102</td>
<td>2</td>
<td>Coplanar (rotated cells)</td>
<td>0.09</td>
</tr>
<tr>
<td>Ref. [23]</td>
<td>2</td>
<td>−1 and +1</td>
<td>96</td>
<td>2</td>
<td>Coplanar (not required)</td>
<td>0.1</td>
</tr>
<tr>
<td>Ref. [24]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>59</td>
<td>1</td>
<td>Coplanar (clocking based)</td>
<td>0.04</td>
</tr>
<tr>
<td>Ref. [25]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>63</td>
<td>0.75</td>
<td>Coplanar (rotated cells)</td>
<td>0.05</td>
</tr>
<tr>
<td>Ref. [26]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>47</td>
<td>1</td>
<td>Coplanar</td>
<td>0.04</td>
</tr>
<tr>
<td>Ref. [27]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>45</td>
<td>0.5</td>
<td>Coplanar (not required)</td>
<td>0.396</td>
</tr>
<tr>
<td>Ref. [28]</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>41</td>
<td>0.5</td>
<td>Coplanar (rotated cells)</td>
<td>0.04</td>
</tr>
<tr>
<td>Proposed full-adder</td>
<td>Without fixed cell</td>
<td>Without fixed cell</td>
<td>40</td>
<td>1</td>
<td>Not required</td>
<td>0.03</td>
</tr>
<tr>
<td>2-input XOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ref. [29]</td>
<td>2</td>
<td>Only −1</td>
<td>32</td>
<td>1</td>
<td>Not required</td>
<td>0.02</td>
</tr>
<tr>
<td>Ref. [30]</td>
<td>2</td>
<td>−1 and +1</td>
<td>32</td>
<td>1</td>
<td>Not required</td>
<td>0.04</td>
</tr>
<tr>
<td>Ref. [31]</td>
<td>3</td>
<td>−1 and +1</td>
<td>13</td>
<td>0.5</td>
<td>Not required</td>
<td>0.12</td>
</tr>
<tr>
<td>Ref. [36]</td>
<td>1</td>
<td>Only +1</td>
<td>55</td>
<td>1</td>
<td>Different phases</td>
<td>0.49</td>
</tr>
<tr>
<td>Proposed XOR</td>
<td>1</td>
<td>Only +1</td>
<td>37</td>
<td>1</td>
<td>Different phases</td>
<td>0.03</td>
</tr>
</tbody>
</table>

Fig. 10. Performance of latency, complexity, area of coplanar one-bit full-adders.

Fig. 11. The proposed 2-input XOR gate (a) the layout (b) the simulation result.

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this tool evaluates the maximum, minimum and average power dissipation occurred in a QCA design under nonadiabatic switching.21

3. A REVIEW OF THE RELATED WORKS
The adder component consists of 3 inputs which include: A, B, and C\textsubscript{in}. The functionality of one-bit full-adder can be given by Eqs. (6) and (7).

\[
\begin{align*}
\text{SUM} &= A \oplus B \oplus C\textsubscript{in} \\
C\text{out} &= (AB + AC\textsubscript{in} + BC\textsubscript{in})
\end{align*}
\] (6) (7)

In general, in QCA field, regarding the 3-input majority gate, it can implement the Carry output \(C\text{out}\) with the least cell consumption on a single layer. Also, the implementation of the sum outputs in general form (using two Exclusive-or gate) which this gate can be implemented with two different approaches. In the first approach, in order to implement, Exclusive-or gate has been used an and/or/inverter gates to implement a full-adder cell. So the formula for Sum, which can be given by Eq. (8)20 has been introduced, as shown below:

\[
\text{Sum} = MV(MV(A, \bar{B}, C\textsubscript{in}), MV(A, B, \bar{C}\textsubscript{in}), MV(\bar{A}, B, C\textsubscript{in}))
\] (8)

Although the SUM formula after being simplified in Ref. [15]. Which has been introduced, are as the following:

\[
\begin{align*}
\text{Sum} &= MV(MV(\bar{A}, \bar{B}, \bar{C}\textsubscript{in}), MV(A, B, \bar{C}\textsubscript{in}), C\textsubscript{in}) \\
&= MV(Carry, MV(A, B, \bar{C}\textsubscript{in}), C\textsubscript{in})
\end{align*}
\] (9)

With the use of Eq. (9), less majority and inverter gates are needed.

In the second approach, in order to implement, SUM part has used a 5-input majority gate. This approach was introduced in Ref. [16]. This proposed approach decreases the latency and area. Although in this paper the first approach is used and we are able to decrease the area compared with the full-adder based on the second approach, the latency of full-adder based on the second approach is still less. The formula for SUM function based on Ref. [16]. Has been introduced in the following:

\[
\text{Sum} = MV(\bar{C}\text{arry}, \bar{C}\text{arry}, C\text{arry}, A, B)
\] (10)

In addition, other QCA full-adder designs are implemented based on the Eq. (10) which are multi-layer structures such as Refs. [17, 18].

3.1. Some of the Popular Adder Designs
In general, there are many famous full-adder designs in QCA field which we present some of them. First, we describe adder design in Ref. [24] which the layout of this design is illustrated in Figure 6(a) and it has been implemented based on Eq. (9). Second, we describe another adder design in Ref. [25] which the layout of this design is shown in Figure 6(b) and it has been implemented based on Eq. (10). The third full-adder which has been presented in Ref. [26], it has been implemented based on Eq. (9). The layout of this design is shown in Figure 6(c). The Forth full-adder as is shown in Figure 6(d) it has been presented in Ref. [27] which it is implemented based on Eq. (10). Fifth, it has been presented a new structure for implementation of the full-adder in Ref. [28] which is shown in Figure 6(e). In order to create this layout, it has been used a 3-input majority and TIEO gates which these two parts with a combination of normal cells and rotated cells are created. In order to decrease some parameters such as cell count, area accusation and power consumption, it is used a number of rotated cells. This method achieves good results for some parameters but it has one important disadvantage about difficulty of realization of rotated cells.24

4. THE PROPOSED FULL-ADDER CELL
As the importance of coplanar designs in QCA technology due to the costly fabrication of multi-layer designs,19

<table>
<thead>
<tr>
<th>Single layer full-adder circuits</th>
<th>Avg. leakage energy dissipation (mev)</th>
<th>Avg. switching energy dissipation (mev)</th>
<th>Avg. energy dissipation of circuit (over all vector pairs)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.5 EK</td>
<td>1 EK</td>
<td>1.5 EK</td>
</tr>
<tr>
<td>Ref. [9]</td>
<td>107.34</td>
<td>290.74</td>
<td>495.26</td>
</tr>
<tr>
<td>Ref. [15]</td>
<td>90.05</td>
<td>240.76</td>
<td>402.05</td>
</tr>
<tr>
<td>Ref. [18]</td>
<td>27.69</td>
<td>84.08</td>
<td>151.39</td>
</tr>
<tr>
<td>Ref. [22]</td>
<td>58.48</td>
<td>58.48</td>
<td>272.29</td>
</tr>
<tr>
<td>Ref. [23]</td>
<td>27.91</td>
<td>85.42</td>
<td>153.58</td>
</tr>
<tr>
<td>Ref. [24]</td>
<td>40.07</td>
<td>118.85</td>
<td>208.7</td>
</tr>
<tr>
<td>Ref. [25]</td>
<td>37.21</td>
<td>98.50</td>
<td>165.04</td>
</tr>
<tr>
<td>Ref. [26]</td>
<td>13.24</td>
<td>41.68</td>
<td>75.06</td>
</tr>
<tr>
<td>Ref. [27]</td>
<td>12.12</td>
<td>37.53</td>
<td>68.16</td>
</tr>
<tr>
<td>Ref. [28]</td>
<td>21.26</td>
<td>62.38</td>
<td>106.89</td>
</tr>
<tr>
<td>Proposed full-adder</td>
<td>13.57</td>
<td>38.79</td>
<td>67.14</td>
</tr>
</tbody>
</table>

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we propose a coplanar full-adder cell which is superior in terms of cell count and area overhead and energy dissipation in comparison to previous designs. The proposed one-bit full-adder cell is shown in Figure 7. This implementation is based on Wang’s full-adder design in Ref. [15]. It consists of three 3-input majority gates and two inverter gates. Moreover, the coplanar clock-phase based approach crossover is used in the proposed structure. The proposed full-adder cell has different delay lines and critical path delay. Respectively the sum delay line is equal to 1 clock (4 clock phase) and carry delay line is equal to 0.5 clock (2 clock phase).

Proposed one-bit full-adder has created many improvements which in simulation part the improvement results are illustrated. Besides, to design a high performance, a low power element has been used. For example, for the implementation of the inverter gate, there are two designs. The structure of each of them is described in Section 2. Moreover, in Table I, the power conception of each of them is illustrated. Beside in Figure 8, the thermal map of

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**Fig. 12.** The energy dissipation thermal maps for the QCA full-adder cells at 2 K with 0.5 EK (a) Ref. [23] (b) Ref. [24] (c) Ref. [25] (d) Ref. [26] (e) Ref. [27] (f) Ref. [28] (g) Proposed work.
Fig. 13. The leakage energy dissipation analysis of the full-adders in diverse tunneling energy levels.

Fig. 14. The switching energy dissipation analysis of the full-adders in diverse tunneling energy levels.

Fig. 15. The average energy dissipation of the full-adders in diverse tunneling energy levels.
Table IV. Energy consumption analysis of XOR gates.

<table>
<thead>
<tr>
<th>Single layer full-adder circuits</th>
<th>Avg. leakage energy dissipation (meV)</th>
<th>Avg. switching energy dissipation (meV)</th>
<th>Avg. energy dissipation of circuit (over all vector pairs)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.5 EK</td>
<td>1 EK</td>
<td>1.5 EK</td>
</tr>
<tr>
<td>Ref. [29]</td>
<td>11.51</td>
<td>31.91</td>
<td>54.60</td>
</tr>
<tr>
<td>Ref. [6]</td>
<td>15.79</td>
<td>48.81</td>
<td>88.26</td>
</tr>
<tr>
<td>Proposed XOR</td>
<td>12.83</td>
<td>36.7</td>
<td>63.5</td>
</tr>
</tbody>
</table>

5. SIMULATION RESULTS AND COMPARISONS

In this section, the proposed full-adder cell is simulated using the QCADesigner version 2.0.3. All of the simulation measurements were set as for default values in QCADesigner. The size of every QCA cell was set to 18 × 18 nm with 5 nm diameter quantum dots. The parameters for bistable approximation are as follows: 0.001 convergence tolerance, 12.9 relative permittivity, 9.8e−22 J clock high, 3.8e−23 J clock low, 11.5 layer separation, and 100 maximum iterations per sample. The simulation results of the proposed full-adder cell is shown in Figure 9. Considering, the examples of Ref. [9], if we set the different polarizations in different wires and after extending any wire with any polarization, then if we use two or more cells, in final point all wires have the same high polarization. As a result, the noise of output cell with the use of this design rule is improved. Moreover, the comparisons of the proposed single layer full-adder and its most efficient counterparts are provided in Table II. Figure 10 illustrates the results of comparison.

Our main purpose is designing a novel efficient full-adder cell. So we use a specific formula that is presented in Ref. [15]. In this formula, full-adder cell creates by combining interaction of same input resources. Hence, we cannot separate them into same gates. But with use of the other general formula of full-adder cell it can create with two independent units. In other words, some units implement with independent XOR and other units implement with an independent majority. So if we want to create a modified XOR based on the used formula in Ref. [15] we cannot show a good new XOR gate. Because our main idea is designing an efficient full-adder and we have focused on this goal. Our proposed coplanar 2-input XOR gate and its simulation result are shown in Figures 11(a) and (b) respectively.

0.5, 1 and 1.5 EK are different surfaces of energy which these surfaces with QCAPro tool have been set a standard and a library of that has been added to this tool.

Moreover, for better analysis and comparison the full-adder energy consumptions have also been calculated using the QCAPro tool, (Table III). Thermal map of the five recent designs and the proposed QCA full-adder cells at 2 K temperature with 0.5 EK are illustrated in Figure 12. Moreover, the energy improvement results are shown in Figures 13–15.

Table III depicts the energy dissipation analysis of the efficient adder cells in three distinct tunneling energy levels (0.5, 1, and 1.5 EK) at 2 K temperature. Considering the results, the proposed design dissipates lower energy as compared to its best previous counterparts. The results indicate that the proposed adder cell leads to almost 15.83% and 23.61% in 1 EK improvements in terms of switching and total energy dissipations as compared to its previous counterparts. Table IV shows the energy consumption analysis of 2-input XOR gates.

The energy dissipation map of the QCA adder cells at 2 K temperature with 0.5 EK is shown in Figure 12. In this figure, the darker cells dissipate higher energy. Clearly, appropriate cell configuration and using the inherent capabilities of QCA cells in the proposed plan have provided this design with the minimum power dissipation as compared to the other adders. In this designs, we are analyzing power consumption of full-adders. Considering our study, two elements have more high impact to increase power consumption. These elements are majority and inverter gates. Since these elements are significant in QCA designs, so we have more calculation process in this point.
6. CONCLUSION
In this study, a novel energy efficient with reduced area single layer full-adder cell in quantum-dot cellular automata was presented. This structure can be used for designing a QCA circuit using one single layer having low energy dissipation. Moreover, the placement of all input and output cells are located on the outsides; thus, a better physical management can be performed. In comparison to the best-published results, the proposed design improved in terms of complexity area and power consumption. Particularly simulation results show 2.43% and 24.24% as well as (27.54% in 0.5, EK, 23.61% in 1 EK and 21.02% in 1.5 EK) reduction respectively in complexity and area overhead as well as power consumption. The simulation results achieved using QCA Designer and QCA Pro tools indicate the superiority of the proposed designs in terms of performance, area and energy dissipation. Finally, a new coplanar 2-input XOR gate based on the proposed full-adder cell was presented.

Acknowledgment: We are grateful to Miss. Bahar Houtan for her language revising on this manuscript and her kindness.

References
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