Designing efficient QCA even parity generator circuits with power dissipation analysis

Ali Newaz Bahar a,*, Muhammad Shahin Uddin b, Md. Abdullah-Al-Shafi c, Mohammad Maksudur Rahman Bhuiyan d, Kawsar Ahmed a

a Department of Information and Communication Technology (ICT), Mawlana Bhashani Science and Technology University (MBSTU), Santosh, Tangail 1902, Bangladesh
b School of Engineering and Information Technology, University of New South Wales, Canberra, Australia
c Institute of Information Technology (IIT), University of Dhaka, Dhaka 1000, Bangladesh
d University Grants Commission of Bangladesh, Dhaka, Bangladesh

Received 9 November 2016; revised 5 February 2017; accepted 13 February 2017

Abstract In the era of modern digital technology, highly scaled and ultra-low power consuming devices have drawn a considerable attention. Quantum-dot Cellular Automata (QCA) are such an emerging nanotechnology that dispenses a highly dense and ultra-low power consuming binary information encoding paradigm. This potential merit instigated the QCA to be an excellent alternative to the conventional Complementary Metal-Oxide-Semiconductor (CMOS) technology. In this paper, we are going to introduce highly scaled and ultra-low power consuming 4, 8, 16 and 32-bit even parity generator circuits. The proposed 4-bit even parity circuit requires 72% fewer cells and occupies 78% less area as compared to previous best designs. Besides, the proposed 32-bit even parity design occupies only 0.283 \text{ \textmu m}^2 whereas the previous best reported design occupies 2.08 \text{ \textmu m}^2 area. The simulation outcomes reveal that our presented designs have considerable enhancements in terms of cell counts, area and power consumption aspects. In addition, to design and verify the proposed layout, QCADesigner is employed and power dissipation is estimated using QCAPro.

1. Introduction

In recent years, CMOS technology runs into numerous designing restrictions in nano-scale computing [1]. Thus, a number of researches have been ascertained to find the suitable substitutes for the classic CMOS technology [1–3]. Quantum-dot cellular automata (QCA) are one of the promising nano-computing technology and potential substitutes of CMOS technology [2,3]. In 1993, C.S. Lent introduced QCA; after that, a number...
Fig. 1  (a) Basic QCA cell with two-type of polarization, (b) two different types of QCA binary wire and (c) different types of QCA inverter.

Fig. 2  (a) Three-input majority voter gate and (b) two different structures of five-input majority voter gate.

Table 1  Truth table of 4-bit even parity generator.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>X_1</th>
<th>X_2</th>
<th>X_3</th>
<th>X_4</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
of QCA based logic circuits, such as memory cells [5–9], adder circuits [10–22] and reversible logic circuits [23–31] have been proposed. In [32], Hashemi et al. introduced the even parity generators which required 168 and 1968 cells to design 4-bit and 32-bit respectively. Another design proposed by Angizi et al. in [33] required 188 and 1862 cells for employing a 4-bit and 32-bit parity generator. For implementing 4-bit even parity generator Sheikhfaal et al. [34] used 98 cells. The most optimized design was proposed by Singh et al. in [35] which required 87 and 1044 cells, respectively, for implementing the 4-bit and 32-bit parity generator.

In this paper, we introduce an innovative design of a 4, 8, 16 and 32-bit parity generator. Moreover, the power consumption of the proposed design has also been calculated. In comparison with previous QCA designs, the proposed layouts are implemented with the minimum area, minimum number of cells and time delays. The rest of the paper is organized as follows: the background of QCA technology is described in Section 2, while Section 3 presents the QCA implementation of proposed circuit. A simulation result is discussed in Section 4. Section 5 inspects power dissipation and finally this paper is concluded in Section 6.

2. QCA background

In QCA technology, QCA cell is the fundamental building block which has four quantum dots with two movable electrons [4]. In a cell, the moveable electrons are located diagonally and are capable of swapping their positions between adjacent dots but not between neighboring cells [4]. Depending on the electron’s position in a cell, a QCA cell can be classified as polarization $P = +1$ (to represent binary “1”) and $P = -1$ (to represent binary “0”) shown in Fig. 1(a). A QCA wire is deployed to transmit the signal by arranging the cell consecu-
tively with the same polarization as shown in Fig. 1(b). When the information passes through a QCA wire, there is no electric current flow between neighboring cells, which leads to ultra-low power consumption [3]. For inverting the signal in QCA, a number of cell arrangements have been reported [2–4] and are shown in Fig. 1(c). The heart of the QCA logic unit is a majority gate or voter (MV) as shown in Fig. 2. There are different types of majority gate such as 3-input majority gate [2–4], 5-input majority gate [17–20], and 7-input majority gate [36].

3. Proposed gates and QCA implementation

In data communication, parity bits are included to data in order to detect transmission errors. A 4-bit even parity generator has four input and one output, and Table 1 represents the truth table. To implement this circuit in QCA, we used a novel 3-input XOR gate [37]. This proposed 4-bit layout uses only 24 cells, occupies 0.022 μm² area and requires two clock cycle to generate the correct output. Fig. 3 presents the QCA block diagram and circuit layout of 4-bit parity generator.

The 8-bit even parity generator has been implemented using only 51 cells and requires only three clock pulses to generate the actual outputs. In Fig. 4, the QCA representation of an 8-bit even parity generator has been shown.

To design a 16-bit parity generator, seven 3-input exclusive-OR and one 2-input exclusive-OR gates are needed. Fig. 5 shows the QCA implementation of a 16-bit parity generator where the input cells are leveled as X₁, X₂...X₁₆ and the output cell is leveled as “Output”.

A 32-bit even parity generator is shown in Fig. 6. This design is required 217 QCA cells and occupied 0.283 μm² area.

4. Simulation result and discussion

Our proposed layout is designed and verified by using QCA-Designer version 2.0.3 [38]. Both Bistable and Coherence Vector simulation techniques are employed with default parameters. Identical outcomes are achieved in both simulations, which ensure the correctness of the proposed design. The simulation results of the proposed 4-bit parity generators are shown in Fig. 7.
Fig. 6  QCA representation of a 32-bit parity generator.

Fig. 7  Simulated input-output waveform of proposed 4-bit parity generator.
A detailed comparison between our proposed parity generator and previously reported design is given in Table 2 with different aspects.

From Table 2, it is evident that our design transcends all the previous designs [32–35] in terms of cell counts, area and delay. Evidently, the proposed 4-bit parity generator needs only 24 cells whereas 87 cells have been used to design in [35]. In contrast, the extremely dense 32-bit parity generator circuit shown in Fig. 7 required only 217 cells with 827 cells optimization in comparison with the earlier best design [35]. It is worth mentioning that this design has a significant improvement in area optimization by saving 1.797 \( \mu m^2 \) covered area upon the design in [35]. In addition, the overall improvement achieved by the proposed design is shown in Fig. 8.

From the above figure, it is expressly notified that our projected 4-bit, 8-bit, 16-bit and 32-bit parity generator circuits are a considerable improvement on all prior design. Evidently, the proposed 4-bit, 8-bit, 16-bit and 32-bit parity generator circuits require 72%, 76%, 80% and 79% less cells respectively, compared to the previous best design [35]. Also, the reported design optimizes 78%, 75%, 82% and 86% area.

### 5. Power dissipation analysis

The power dissipation by QCA cell is calculated using the upper bound power dissipation model [39–42] is given as

\[
P_{\text{diss}} = \frac{E_{\text{diss}}}{T_{\text{cc}}} \left( \frac{\hbar}{2T_{\text{cc}}} \right) \times \left[ \frac{T}{|T|} \tanh \left( \frac{\hbar \Gamma_{+}}{k_B T} \right) + \frac{T}{|T|} \tanh \left( \frac{\hbar \Gamma_{-}}{k_B T} \right) \right]
\]

In order to calculate the power dissipation of proposed parity generator, we employed QCAPro [43]. The power dissipation is measured in different tunneling energy levels at 2 K temperature, described in Table 3. In addition, the average leakage energy, average switching energy and average energy dissipation at three separate tunneling energy levels of proposed design and earlier reported designs are illustrated in Fig. 9.

### 6. Conclusions

In this paper, different bit length parity generators have been introduced. The proposed 4-bit parity generator occupies only a 0.022 \( \mu m^2 \) area whereas the previous best circuit [35] occupied a 0.10 \( \mu m^2 \) area. Our proposed 4-bit circuit requires 72% less cells compared to [35]. Similarly, our proposed 8-bit, 16-bit and 32-bit parity generator circuit achieved remarkable improvement over the earlier design [32–35]. In addition, the energy dissipation of the proposed design has been investigated using QCAPro tools. Finally, the results ensure the superiority of our design over prior designs in terms of cell count, occupied area, time delay and energy dissipation.
Fig. 8 Overall improvement achieved by the proposed (a) 4-bit parity generator, (b) 8-bit parity generator, (c) 16-bit parity generator and (d) 32-bit parity generator over the previous design.
Table 3  Energy dissipation analysis of parity generators.

<table>
<thead>
<tr>
<th>Circuits</th>
<th>Leakage energy dissipation (MeV)</th>
<th>Switching energy dissipation (MeV)</th>
<th>Total energy dissipation (MeV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.5 $E_k$</td>
<td>1.0 $E_k$</td>
<td>1.5 $E_k$</td>
</tr>
<tr>
<td>4-bit parity generator</td>
<td>3.77</td>
<td>12.53</td>
<td>23.96</td>
</tr>
<tr>
<td>8-bit parity generator</td>
<td>6.65</td>
<td>22.35</td>
<td>39.81</td>
</tr>
<tr>
<td>16-bit parity generator</td>
<td>13.03</td>
<td>41.95</td>
<td>79.64</td>
</tr>
<tr>
<td>32-bit parity generator</td>
<td>29.67</td>
<td>94.72</td>
<td>165.31</td>
</tr>
</tbody>
</table>

Fig. 9  The (a) average leakage energy dissipation, (b) average switching energy dissipation and (c) total energy dissipation at three different tunneling energy levels ($T = 2.0$ K).
References


Please cite this article in press as: A.N. Bahar et al., Designing efficient QCA even parity generator circuits with power dissipation analysis, Alexandria Eng. J. (2017), http://dx.doi.org/10.1016/j.aej.2017.02.002.


