Area Efficient Magnitude Comparator
Based on QCA

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Abstract. In this paper, the logic design of 1-bit comparator based on the Quantum-Dot Cellular Automata (QCA) is presented. QCA is an engaging innovation outlining extremely stubby power and high reaction digital circuits. QCA is a computational model of Quantum hypothesis. QCA viably conquers the scaling deficits of CMOS innovation. In the outline of digital logic, a comparator is the basic forming segment which executes the similarity of two numbers. The proposed design is altogether declined regarding the area and cell complexity, surveyed to other designs and time cycle is retained at least. Power usage of the proposed circuit is evaluated and compared, that demonstrates the proposed QCA design have lesser power consumption to regular outlines. The proposed comparator required 57.2% less area and dispersed 52% less energy. The proposed circuit has been confirmed and simulated utilizing QCADesigner and QCAPro has been utilized to gauge the power dispersal.

1 Introduction

QCA is a standout amongst the most encouraging options of CMOS in the field of nanoscience for low power utilization and fast operation in future generation computer. The extent of the transistor diminishment has been the significant pattern to accomplish circuits fast quick speed, high density and low power dissemination. QCA as emerging innovation past current transistor changes to encode binary information. Quantum dots are nanostructures made from standard semi conductive materials. These structures are displayed as quantum wells. They show energy impacts even at distances a few hundred times than the material system lattice constant. A dot can be imagined as well. When electrons are caught inside the dot, it requires higher energy for electron to get away. QCA is a novel innovation that endeavors to make general computational usefulness at the Nano scale by controlling the position of single electrons. This innovation guarantees low energy dispersal with higher speed and parallel processing capacity at Nano-scale level. Its essential building block is a cell made out of four dots, works by changing the position of two electrons. There's two conceivable course of action of a cell as two electrons situated corner to corner for columbic repulsion force. Essential logic gates can be planned by masterminding these cells in various ways. \([1], [2]\)

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In this work, QCA comparator design is proposed which has been additionally stretched out to plan 1-bit comparator circuit. The robustness of the proposed 1-bit comparator circuit has been likewise confirmed to check the reproducibility and power efficiently in order to comprise further large scale layouts.

2 Proposed Comparator

A new highly area efficient coplanar QCA 1-bit comparator design is proposed in this section. The schematic of the proposed coplanar 1-bit comparator is shown in Fig. 1(a). The Comparator is a combinational circuit which finishes the appraisal of two numbers and demonstrates if any of them is equivalent to, more greater than, or not as much as another number [3]. The fundamental segment of a 1-bit comparator is two input lines alongside three relating outputs. As indicated by the Fig 1(b), it takes two inputs A, B and they are correctly distinguished though they are equivalent (A=B), greater (A>B) or lesser (A<B) than the particular rival bit. The 1-bit comparison can be computed as Eq. (1).

Our proposed design is obtained by three basic logic gates AND, XOR and invert operation. We have used one of efficient and compact XOR gate [4]. In addition for invert operation we use QCA rotated cell based inverter gate. Especially, this inverter simply uses two offset and rotated cells to reverse the signal traversing the wire. By using robust XOR and rotated cell based inverter we have found an optimal way to design complex QCA structures which reduces circuit complexity with no wire crossing. This layout entails the lowest number of cells and less area as compared to the previous works. The proposed 1-bit comparator takes 85 QCA cell with a region of 0.06μm². Regardless of allowing the substantially united QCA designs, not any of the multi-layer technique is operated to permeate the difficulties of wire crossing methods.

\[
\begin{align*}
A < B &= \overline{AB} \\
A &= B = AB + \overline{AB} \\
A > B &= A\overline{B}
\end{align*}
\]

(1)

Fig. 1. (a) schematic diagram of 1-bit comparator, (b) QCA implementation of 1-bit comparator, (c) simulation result of 1-bit comparator
The power utilization of proposed 1-bit comparator is examined with the assistance of QCAPro tool [5] which evaluates the power dispersal of the QCA structures at 2 K temperature under the three diverse energy levels (0.5Ek, 1.0Ek, 1.5Ek).

### Table 1. Comparison of energy dissipation results of 1-bit Comparator.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$\gamma=0.5\text{Ek (meV)}$</th>
<th>$\gamma=1.0\text{Ek (meV)}$</th>
<th>$\gamma=1.5\text{Ek (meV)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6]</td>
<td>660.5</td>
<td>762.8</td>
<td>-</td>
</tr>
<tr>
<td>[8]</td>
<td>380.8</td>
<td>415.6</td>
<td>-</td>
</tr>
<tr>
<td>Proposed</td>
<td>182</td>
<td>245.4</td>
<td>320.4</td>
</tr>
</tbody>
</table>

As mentioned before, QCAPro tool as a satisfactory energy estimator tool is used to analyze leakage, switching, and average energy dissipation of the circuits. Table 1 portrays the energy dispersal examination of high performance 1-bit comparator cells in three distinct tunneling vitality levels at 2 K temperature. The power scattering map of our proposed circuit at 2 K temperature with 0.5 Ek is represented in Fig. 0. In this figure, the darker the cells are, the more energy disperses. According to Table 3, it is worth to mention that the proposed 1-bit comparator design dissipates 52% less average energy than previous best design in [8] at 0.5Ek tunneling level.

### 3 Comparison and Performance Analysis

The proposed design of 1-bit comparator was simulated and checked utilizing QCADesigner ver. 2.0.3, a typical and effective tool for QCA gadget tool. The power dissemination is assessed utilizing QCAPro simulator as an exact power estimator device. The simulation result of the proposed 1-bit comparator is shown in Fig. 1(c). The result confirms that the expected output of the proposed design is achieved correctly. Table 2 demonstrates a comparison of the 1-bit comparator in terms of performance metrics number of majority gates, number of inverters, number of wire-crossings, QCA cells, occupied area and delay. As it is clear from the outcomes, the proposed 1-bit comparator has noteworthy improvements contrasted with the past 1-bit comparators. The quantity of cells is dropped in proposal outline. The low number of cells has advantages for examples bring down power utilization, bring down delay and lower occupied area. The quantity of utilized cells in proposed design is 85, while this number in [6] is 319 that have a 73% improvement. Additionally, the quantity of clock zones has enhanced in the proposed design. Decreasing the quantity of clock zones is essential, particularly in large circuits. In view of results, it has 37.5% improvement contrasted with [7]. Occupied area is diminished in proposal design. This improvement is 57.2% compared to [10].
Table 2. Comparison results for comparators.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Nº majority gates</th>
<th>Nº inverters</th>
<th>Nº wire crossings</th>
<th>QCA cells</th>
<th>Area (µm²)</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6]</td>
<td>17</td>
<td>14</td>
<td>6</td>
<td>319</td>
<td>0.343</td>
<td>4</td>
</tr>
<tr>
<td>[7]</td>
<td>5</td>
<td>7</td>
<td>6</td>
<td>223</td>
<td>0.21</td>
<td>2</td>
</tr>
<tr>
<td>[8]</td>
<td>8</td>
<td>7</td>
<td>0</td>
<td>117</td>
<td>0.182</td>
<td>1</td>
</tr>
<tr>
<td>[9]</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>100</td>
<td>0.13</td>
<td>1</td>
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<tr>
<td>[10]</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>97</td>
<td>0.14</td>
<td>1</td>
</tr>
<tr>
<td>Proposed</td>
<td>2</td>
<td>3</td>
<td>0</td>
<td>85</td>
<td>0.06</td>
<td></td>
</tr>
</tbody>
</table>

4 Conclusions

This paper presents design and performance analysis of a new efficient 1-bit comparator design. The proposed QCA comparator design has been functionally verified using QCA designer tool and energy dissipation computations have been performed using QCAPro tool. The proposed 1-bit comparator design utilizes two majority gates, three inverters and XOR gate only. The proposed design demonstrates significantly more robust than the previous 1-bit comparators. Improving the robustness of the 1-bit comparator leads to efficient designing of many arithmetic circuits. The comparison results indicate that the proposed 1-bit comparator achieves considerable improvements over the previous designs in terms of cell count, area and delay. A detailed power consumption comparison was also performed between our proposed circuit and prior designs. The results confirmed the dominance of our design over state-of-the-art design in term of power consumption. In future works, the high robustness of this design can be leveraged to yield the most commonly utilized digital circuits.

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References